## U.S. Patent Application Serial No. 09/749,590

a gate electrode formed above the silicon substrate between the pair of impurity diffused regions with a gate insulation film interposed therebetween, the gate electrode being formed of a first polycrystalline silicon film formed on the gate insulation film, a second polycrystalline silicon film formed on the first polycrystalline silicon film having a thickness of 2-20 nm and thinner than that of the first polycrystalline silicon film and having crystal grain boundaries which are discontinuous to the first polycrystalline silicon film, and a metal nitride film formed on the second polycrystalline silicon film.

2. (Twice Amended) A semiconductor device comprising:

a pair of impurity diffused regions formed in a silicon substrate, spaced from each other; and a gate electrode formed above the silicon substrate between the pair of impurity diffused regions with a gate insulation film interposed therebetween, the gate electrode being formed of a first polycrystalline silicon film formed on the gate insulation film, a second polycrystalline silicon film formed on the first polycrystalline silicon film having a thickness of 2-20 nm and thinner than that of the first polycrystalline silicon film and having crystal grain boundaries which are discontinuous to the first polycrystalline silicon film, a metal nitride film formed on the second polycrystalline silicon film, and a metal film form on the metal nitride film.

 $G_{\boldsymbol{\theta}}$ 

3. (Amended) A semiconductor device according to claim 1, wherein a native oxide film or a chemical oxide film formed by liquid chemical treatment is formed between the first polycrystalline silicon film and the second polycrystalline silicon film.

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cover.

4. (Amended) A semiconductor device according to claim 2, wherein a native oxide film or a chemical oxide film formed by liquid chemical treatment is formed between the first polycrystalline silicon film and the second polycrystalline silicon film.